BF909; BF909R

N-channel dual gate MOS-FETs

Rev. 02 — 19 November 2007 Product data sheet

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NXP Semiconductors

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N-channel dual gate MOS-FETs BF909; BF909R

FEATURES

- Specially designed for use at 5 V supply voltage
- High forward transfer admittance
- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

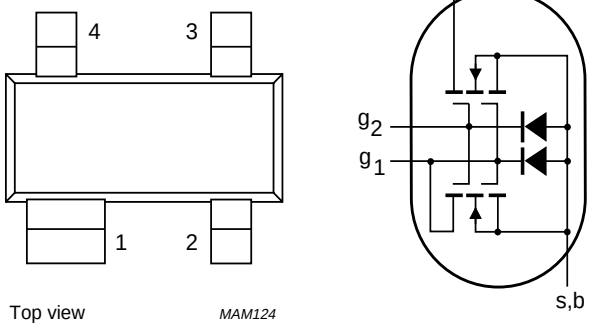
DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143 or SOT143R package. The transistor consists of an amplifier MOS-FET with source and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

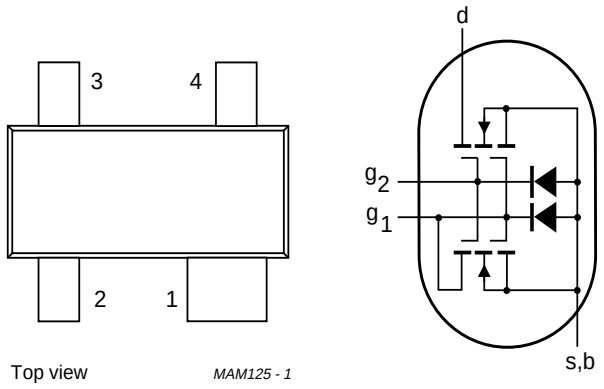
PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g_2	gate 2
4	g_1	gate 1



BF909 marking code: %M3.

Fig.1 Simplified outline (SOT143) and symbol.



BF909R marking code: %M4.

Fig.2 Simplified outline (SOT143R) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	7	V
I_D	drain current		–	–	40	mA
P_{tot}	total power dissipation		–	–	200	mW
T_j	operating junction temperature		–	–	150	°C
$\lvert y_{fs} \rvert$	forward transfer admittance		36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1		–	3.6	4.3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz	–	2	2.8	dB

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	40	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation	see Fig.3			
	BF909	up to T_{amb} = 50 °C; note 1	–	200	mW
	BF909R	up to T_{amb} = 40 °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

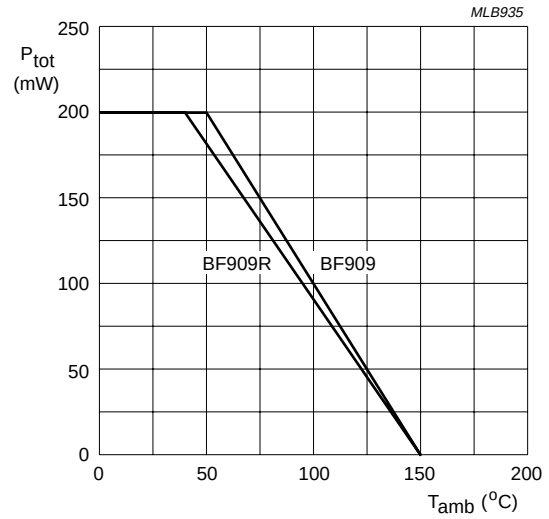


Fig.3 Power derating curves.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	note 1		
	BF909		500	K/W
	BF909R		550	K/W
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point	note 2		
	BF909	T_s = 92 °C	290	K/W
	BF909R	T_s = 78 °C	360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1\text{-}SS}$	gate 1-source breakdown voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{G1\text{-}S}$ = 10 mA	6	15	V
$V_{(BR)G2\text{-}SS}$	gate 2-source breakdown voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{G2\text{-}S}$ = 10 mA	6	15	V
$V_{(F)S\text{-}G1}$	forward source-gate 1 voltage	$V_{G2\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G1}$ = 10 mA	0.5	1.5	V
$V_{(F)S\text{-}G2}$	forward source-gate 2 voltage	$V_{G1\text{-}S}$ = V_{DS} = 0; $I_{S\text{-}G2}$ = 10 mA	0.5	1.5	V
$V_{G1\text{-}S(th)}$	gate 1-source threshold voltage	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; I_D = 20 μA	0.3	1	V
$V_{G2\text{-}S(th)}$	gate 2-source threshold voltage	$V_{G1\text{-}S}$ = V_{DS} = 5 V; I_D = 20 μA	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2\text{-}S}$ = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	12	20	mA
$I_{G1\text{-}SS}$	gate 1 cut-off current	$V_{G1\text{-}S}$ = 5 V; $V_{G2\text{-}S}$ = V_{DS} = 0	–	50	nA
$I_{G2\text{-}SS}$	gate 2 cut-off current	$V_{G2\text{-}S}$ = 5 V; $V_{G1\text{-}S}$ = V_{DS} = 0	–	50	nA

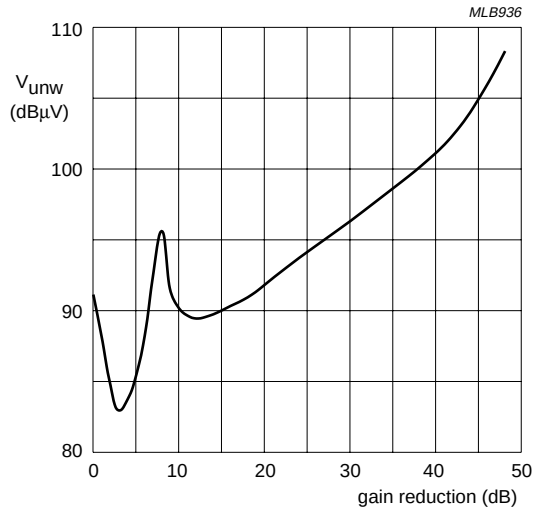
Note

1. R_{G1} connects gate 1 to V_{GG} = 5 V; see Fig.18.

DYNAMIC CHARACTERISTICS

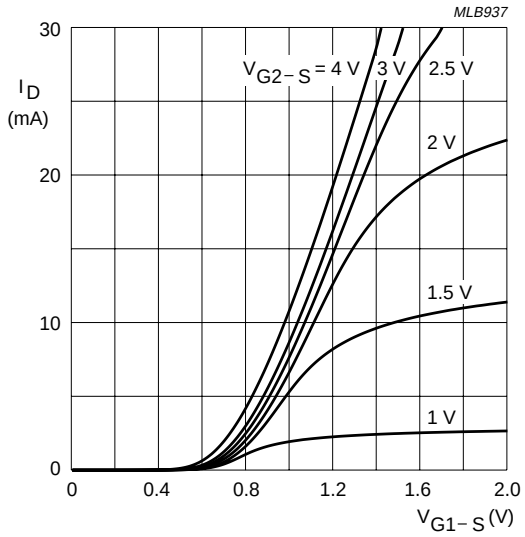
Common source; T_{amb} = 25 °C; V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 15 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	36	43	50	mS
$C_{ig1\text{-}s}$	input capacitance at gate 1	f = 1 MHz	–	3.6	4.3	pF
$C_{ig2\text{-}s}$	input capacitance at gate 2	f = 1 MHz	–	2.3	3	pF
C_{os}	drain-source capacitance	f = 1 MHz	–	2.3	3	pF
C_{rs}	reverse transfer capacitance	f = 1 MHz	–	35	50	fF
F	noise figure	f = 800 MHz; G_S = G_{Sopt}; B_S = B_{Sopt}	–	2	2.8	dB



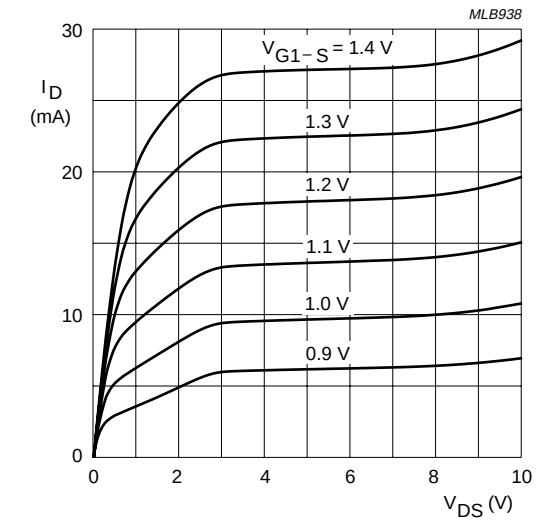
V_{DS} = 5 V; V_{GG} = 5 V; f_w = 50 MHz.
f_{unw} = 60 MHz; T_{amb} = 25 °C; R_{G1} = 120 kΩ.

Fig.4 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.18.



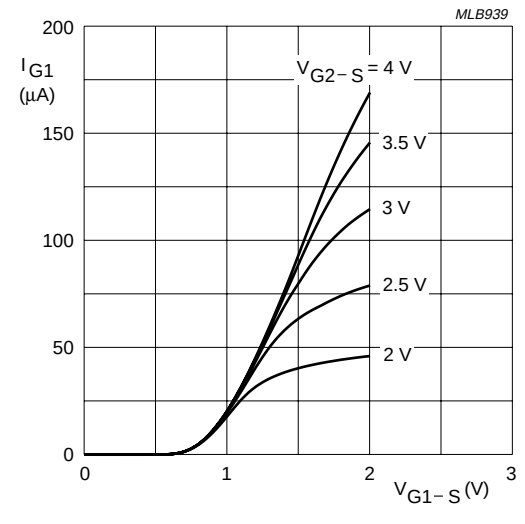
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



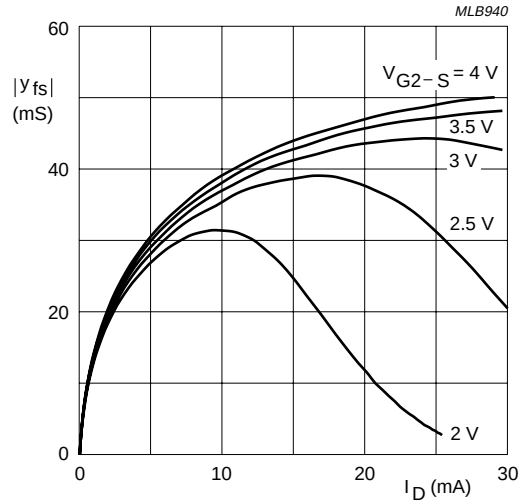
V_{DS} = 5 V.
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



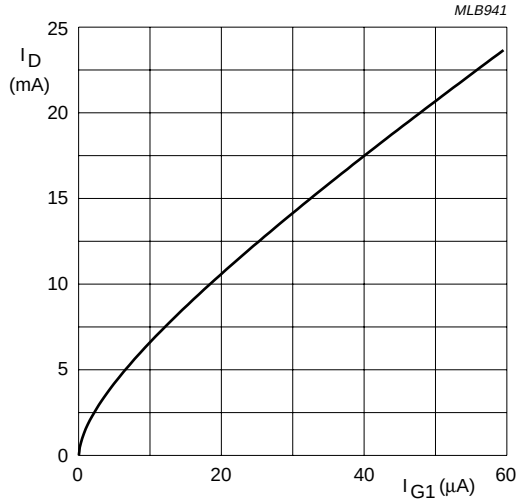
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



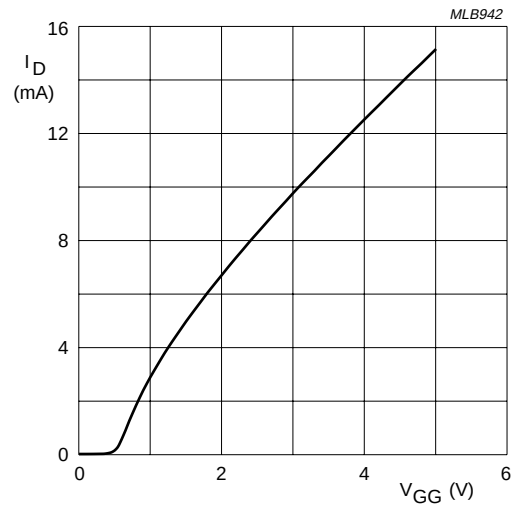
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



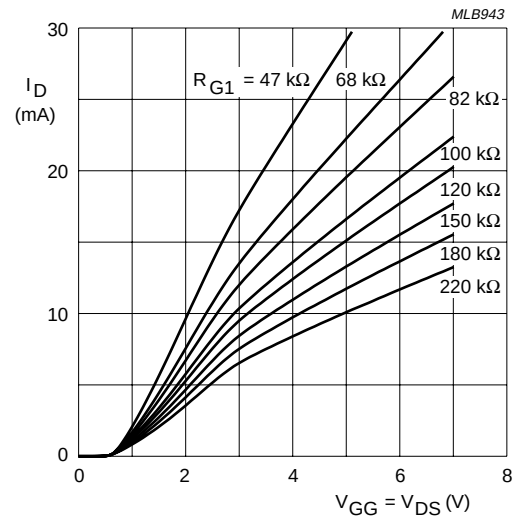
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



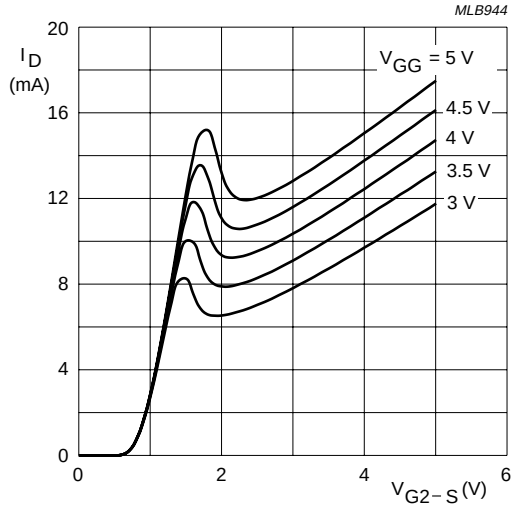
V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V.
R_{G1} = 120 kΩ (connected to V_{GG}); T_j = 25 °C.

Fig.10 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.18.



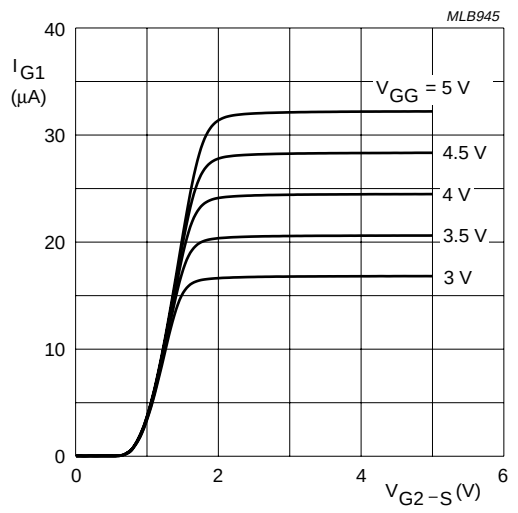
$V_{G2\text{-}S}$ = 4 V.
R_{G1} connected to V_{GG}; T_j = 25 °C.

Fig.11 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.18.



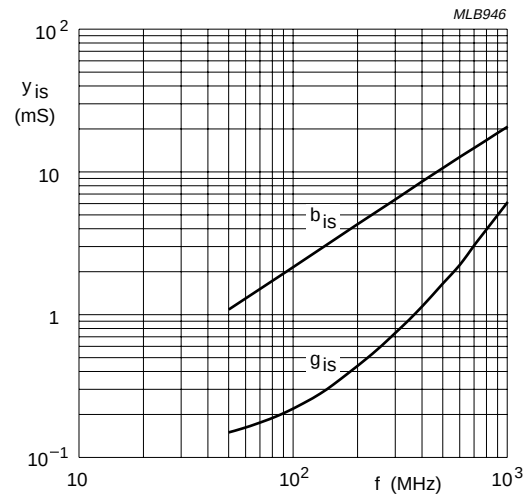
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.12 Drain current as a function of gate 2 voltage; typical values; see Fig.18.



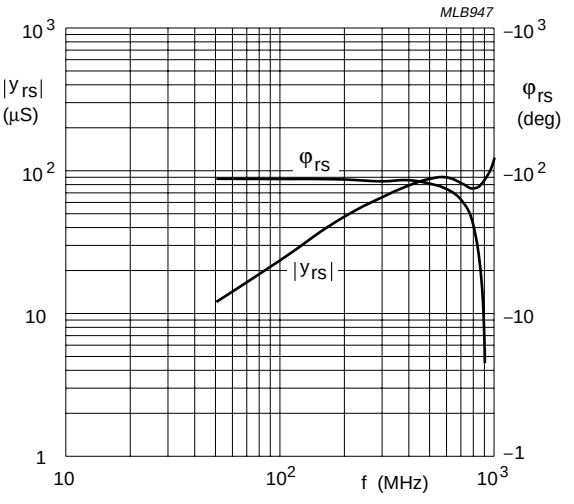
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}).

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.18.



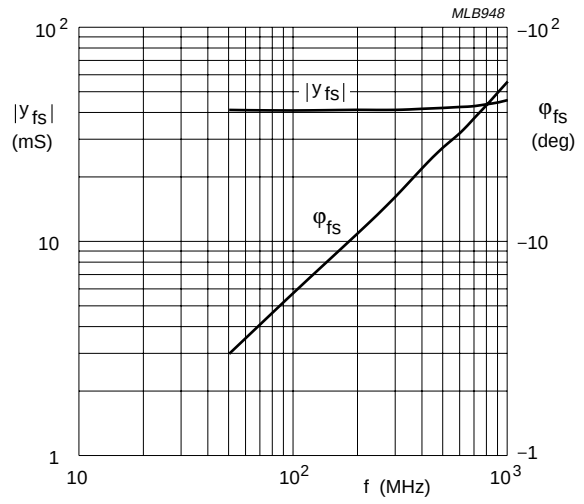
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.14 Input admittance as a function of frequency; typical values.



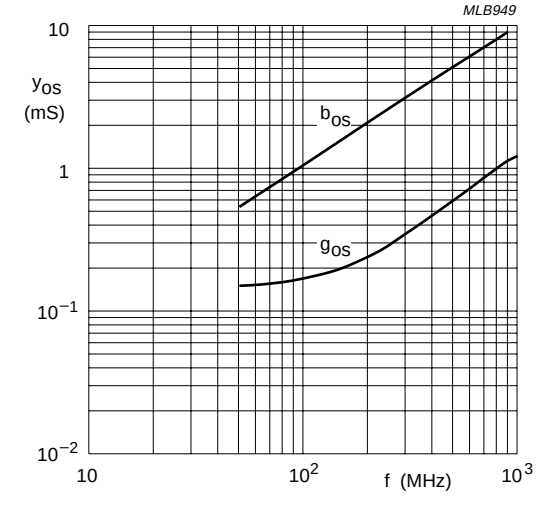
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.15 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.16 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 15 mA; T_{amb} = 25 °C.

Fig.17 Output admittance as a function of frequency; typical values.

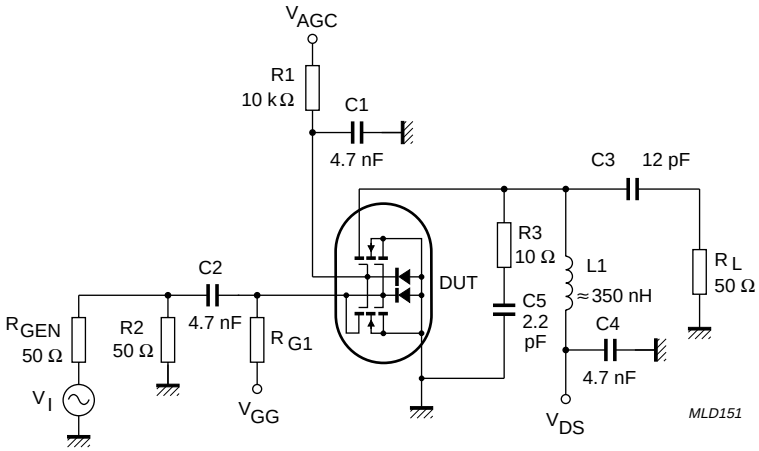


Fig.18 Cross-modulation test set-up.

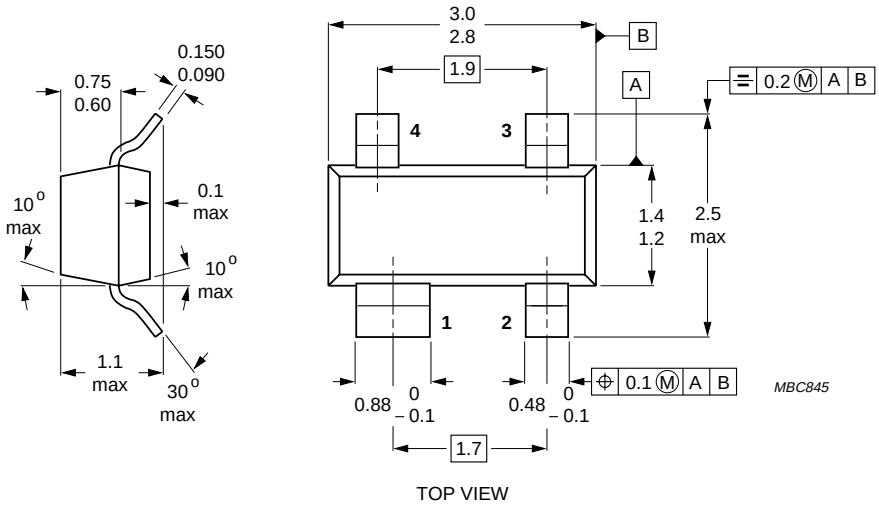
Table 1 Scattering parameters: T_{amb} = 25 °C; V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA

f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.985	–6.4	4.064	172.3	0.001	86.9	0.985	–3.2
100	0.978	–12.6	3.997	164.9	0.002	82.7	0.982	–6.4
200	0.957	–25.0	3.886	150.8	0.005	74.3	0.973	–12.6
300	0.931	–36.5	3.682	137.3	0.006	68.9	0.960	–18.6
400	0.899	–47.6	3.484	123.8	0.007	59.6	0.947	–24.2
500	0.868	–57.4	3.260	111.7	0.007	57.9	0.936	–29.6
600	0.848	–66.6	3.053	101.0	0.006	58.5	0.927	–34.8
700	0.816	–74.6	2.829	90.3	0.005	65.5	0.919	–39.8
800	0.792	–82.2	2.652	79.9	0.005	83.3	0.913	–44.6
900	0.772	–89.3	2.470	69.5	0.005	114.9	0.910	–49.5
1000	0.754	–95.6	2.328	59.5	0.006	138.7	0.909	–54.6

Table 2 Noise data: T_{amb} = 25 °C; V_{DS} = 5 V; V_{G2-S} = 4 V; I_D = 15 mA

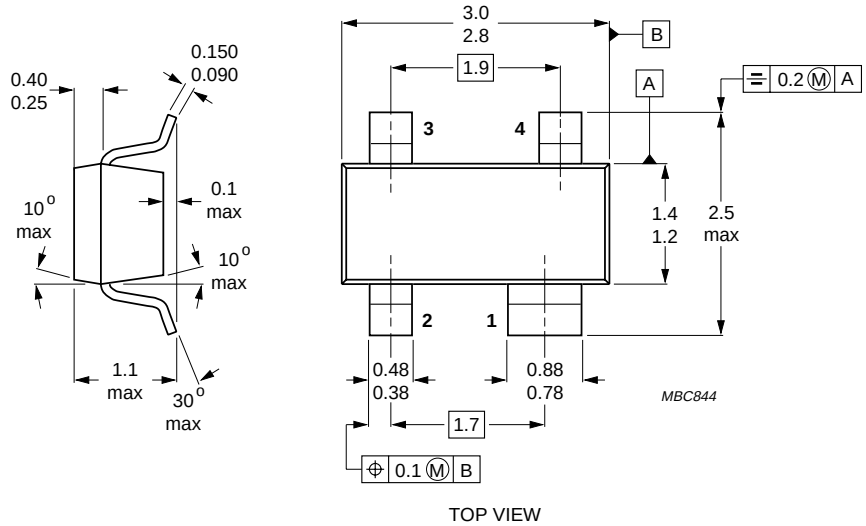
f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.603	67.71	0.581

PACKAGE OUTLINES



Dimensions in mm.

Fig.19 SOT143.



Dimensions in mm.

Fig.20 SOT143R.

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Revision history

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BF909_N_2	20071119	Product data sheet	-	BF909_1
Modifications:	• Fig.1 and 2 on page 2; Figure note changed			
BF909_1	19950425	Product specification	-	-

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